

**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

**Mapping of PO’s and PSO’s through Project**

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| **Title of the Project** | **Design and Implementation of Low Power Decoder using GDI IN 90nm Technology** | |
| **Student Details** | **Roll number** | **Name of the Student** |
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ABSTRACT:

The project's focus is on developing a low-power decoder, a crucial component of modern integrated circuits. The primary objective is to enhance the decoder's design to reduce power consumption while maintaining high performance and scalability. Various VLSI design styles are explored, including CMOS, Transmission Gate Logic (TGL), Pass-transistor Dual-Value Logic (PDVL), and Gate Diffusion Input (GDI). The proposed GDI-based logic decoder significantly reduces transistor count, leading to lower power consumption compared to mixed logic designs. Cadence (Virtuoso) simulation at 90nm is used to implement the GDI decoder, demonstrating reductions in power dissipation compared to typical CMOS and existing mixed logic designs.

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| **PO’s & PSO’s** | **PO 1** | **PO 2** | **PO 3** | **PO 4** | **PO 5** | **PO 6** | **PO 7** | **PO 8** | **PO 9** | **PO 10** | **PO 11** | **PO 12** | **PSO 1** | **PSO 2** |
| **Mapping** | **🗸** | **🗸** | **🗸** | **🗸** | **🗸** | **🗸** | **🗸** | **🗸** | **🗸** | **🗸** | **🗸** | **🗸** | **🗸** | **🗸** |
| **Attainment Level** | 3 | 3 | 3 | 3 | 3 | 2 | 2 | 3 | 3 | 3 | 3 | 2 | 3 | 3 |